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EXAMINER	
SAXENA, AKASH	
ART UNIT	PAPER NUMBER
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/942,096	EL ATA, NABIL A. ABU	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,9-15 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-15 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-5, 9-15, and 19-23 has/have been presented for examination based on amendment filed on 2nd November 2006.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2nd November 2006 has been entered.
3. Claim(s) 1-5,9-12, 19-23 is/are amended.
4. Claim(s) 6-8, 16-18 and 24 is/are cancelled.
5. All rejections presented previously are withdrawn and new ones are explicitly made in this action.
6. Examiner withdraws the USC § 112¶1st rejection pertaining to improper incorporation in view of applicant's argument in remarks submitted on 10th October 2006.
7. The arguments submitted by the applicant have been fully considered. Claims 1-5, 9-15, and 19-23 remain rejected and this action is made NON-FINAL. The examiner's response is as follows.

Response to Applicant's Arguments regarding 35 USC 103

8. Applicant's arguments are moot in view of amended claims but examiner has taken them into consideration in responding to the amended claims. Please see claim interpretation section for application bus and technology bus.

9. Applicant's comments regarding the combination of EUROEXPERT-White-Hartley misses the use of modeled performance metrics during the construction of the proposed information system architecture. Examiner respectfully disagrees as White suggests selecting from the modeled performance metrics (White: Pg.34 Col2 Lines 1-3).

Claim Interpretation In response to the amendment

10. Applicant has disclosed following limitations in claim 1.

> "wherein the constructed proposed information system architecture comprises a technology bus, the technology bus serving as an abstract interface for data access or technology services between the components modeled in the application and technology layers,"

Support for which is found in the specification on Pg.13 Lines 3-13:

> A technology bus layer 440 isolates the technology layer 450 from the application layers 410, 430, avoiding a technology-specific architecture. According to one embodiment, the technology bus layer 440 models an abstract interface (e.g., JavaTM virtual machine) for data access or technology services. By incorporating a technology bus layer 440 into the model, the resulting system architecture is not proprietary to a specific set of hardware components. Thus, portability is maximized with the technology bus layer 440, such that physical hardware in the technology layer 450 may be substituted without requiring substantial porting of code to new hardware platforms. In addition, the technology bus layer 440 provides level compensation, network protocol translators, cryptography, and connection management services.

Examiner has interpreted as one possible embodiment of technology bus to be the virtual machine.

Further the claim discloses,

> "and wherein the constructed proposed information system architecture further comprises an application bus, the application bus providing a communication, distribution, and management interface between application component models in the application layer;"

Support for which is found in the specification on Pg.12 Lines 5-18:

> An application bus layer 420 facilitates the separation of the business applications and application services layers 410, 430, by providing a number of communication services. All communication between software components in both layers 410, 430 must be requested through the application bus layer 420. The communication services modeled may include code and network communication protocol translation services (e.g., Java to Cobol; TCP/IP to SNA), distribution services (e.g., distributing workload to prevent server overload), event, system, and transaction management services (e.g., providing order and integrity for multiple service requests at each level), security services (e.g., authentication), scripting flow, conflict solving, lock processing, and scheduling and dispatching of service requests. Such communication services are modeled as delays or locks, which affect the overall performance metrics of the information system. According to one embodiment, the application bus layer 420 models a communication middleware, such as messaging and TCP/IP network communication protocols.

Examiner has interpreted application bus to be the messaging layer.

11. Claim 21 seems to recites the limitations in means plus function format, however no support from specification is presented. Examiner respectfully requests applicant to present support for each means plus function limitation from the specification.

Claim Rejections - 35 USC § 112¶2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-5, 9-15, and 19-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1

Claim 1 discloses, "constructing the proposed information system architecture". It is unclear if the constructing entails actually physically constructing the information system or is limited to making a plan of the information system architecture.

The indefinite seems to stem from the limitation where "constructing comprises mapping each business process to an application component (**model**)...".

(a) The newly amended limitation, requiring "constructing the proposed system architecture", and the further details of such construction are absent from the specification.

(b) Arguendo, even if the "constructing the proposed system architecture" is read as "constructing a model of the proposed system architecture", which seems to be a multi-layered mathematical model, specification lacks any details how such a multilayered mathematical model should be constructed. While the specification goes into details of mapping each layer to a mathematical model there is no disclosure how such models should be constructed and interfaced.

Due to the above reasons the specification is deficient and would not allow one to make or use the claimed invention.

Independent claims present similar limitations and respective dependent claims also do not clear the indefiniteness. Hence claims 2-5, 9-15, and 19-23 are rejected for reasons above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. **Claim(s) 6-20 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over EUROEXPERT - Best Practices: French Social Security - UNEDIC dated 1992 (EUROEXPERT hereafter), in view of IEEE article – "An Introduction To Six Sigma With Design Example" by Robert White dated 1992 (White hereafter), further in view of US Patent 6532465 issued to Hartley (Hartley hereafter).**

Regarding Claim 1

EUROEXPERT Best Practices document teaches

> ***"A computer implemented method for designing and constructing a model based information system architecture, the information system architecture being the architecture of an information system which includes a number of interconnected hardware and software components implementing one or more business solutions, comprising the steps of:***
> ***(a) providing a business process design, the business process design describing a plurality of business processes and defining a set of business requirements for each business process;***
> ***(b) using a multi-layer mathematical model of a proposed information system architecture supporting the business process design, constructing the proposed information system, the layers of the multi-layer model comprising a business layer, an application layer, and a technology layer, the business layer, application layer and technology layer having different data than each other,"***

as a tiered model GATE model identical to claimed model application that collects measurements from 3 domains, namely, business domain/layer, application domain, technology/system/network domain, illustrated by a figure called "Modeling Business Value Chain" (EUROEXPERT Best Practices: Col 2), *representing an* ***information system*** *(EUROEXPERT: Fig on Pg.2) where each layer has different data than each other (EUROEXPERT: Fig on Pg.1)*. This model incorporates the business goals and characteristics of the system design. It can be seen from the reference that this model captures the business requirements for business processes as well as delegates them to 3 layers. The public knew about this model in February 1992

(EUROEXPERT Best Practices: Col 2, Lines 16-18). EUROEXPERT teaches constructing such a system ((EUROEXPERT: Approach Col 2 – Stage 2 completed in May 1992).

Although the EUROEXPERT Best Practices article discloses the results of the 3-tiered business model, EUROEXPERT does not teach specifically modeling the performance matrix of the for each layer, simulating, comparing them to the requirements, acceptability, proposing & modifying the matrix at appropriate layers.

White's article teaches how six-sigma methodology can be used to perfect any process, system or component. This process has its mathematical roots in statistics. The process itself has six steps, namely, identify the required function, specify performance requirements, determine component variation, characterize performance and revise design to meet six-sigma mathematical requirement, repeat previous steps to get higher quality results (White: Pg 32, Col. 2, Design Example). White further teaches,

> ***"(c) during the construction, modeling performance metrics for each layer of the multi-layer model including continuous service of the proposed information system architecture"***

as the components and their variations can be modeled using an electrical circuit example (White: Pg 33, Col. 1, D Step 3, Line 3-8; During construction – Pg. 35 Section H). These components can then be simulated to measure their performance using various mathematical & statistical calculation, White discloses circuit example with Monte Carlo simulation (White: Pg 33, Col 2, 2nd Paragraph).

White further teaches,

> ***"(d) comparing the modeled performance metrics with the set of business requirements for each business process, said comparing producing respective indications of unacceptable***

performance metrics of one or more business processes that do not satisfy the set of business requirements defined for them based on the produced indications;"

as results of such a simulation are compared against the expected values (White: Pg 34, Col. 1, 1-6 & Figure 4). The figure (White: Figure 4) disclosed shows the unacceptable performance as compared to the expected results.

White further teaches,

"(e) and determining modifications to proposed information the system architecture as being constructed, resulting in an information system architecture design, a description of the resulting information system architecture design being output."

as replacing the instant model and taking other models & values for the sub-components to enhance and meet performance (White: Pg 34, Col. 1, F Step 5, Line 1-8 & Table V). Modifications are suggested after the results from these simulations are gathered – i.e., in the circuit example used components of higher tolerances are suggested (White: Pg 34, Col. 1, F Step 5, Line 15-16). The reference teaches narrower versions of broader claims in the application. Here a simple electric circuit example teaches a abstract methodology that can be applied to much bigger multi-tiered system as claimed. The newly amended limitation adds the outputting the design, which EUROEXPERT teaches as stage 2 implementation of the model (EUROEXPERT: Pg.1, Fig. On Pg.2 New functional Elements).

Neither EUROEXPERT nor White explicitly teaches mapping between the 3 GATE domain layers and presence of application and technology buses in the design.

Hartley teaches the limitation

(a) ... said constructing comprising mapping each business process to an application component which is modeled by a corresponding application component model in the application layer, each application component model linked to one or more component models in the application and technology layers, which support the corresponding application component,

as mapping between the different layers can be present attain a business objective (Hartley: Col. 5 Lines 12-32, also see Fig.4; Col.11 Lines 34-45). Hartley exemplifies the mapping between the presentation layer and business later in his Figure 4 (Hartley: Col 10, Lines 50-55, Lines 64-67). But it can be seen in Figure 4 that similar mapping existing between the layers below the business layer going down towards domain (application layer) and database (physical database/technological representation layer) (Hartley: Col. 8 Lines 11-16). Hartley further teaches the limitation

(a) ... wherein the constructed proposed information system architecture comprises a technology bus, the technology bus serving as an abstract interface for data access or technology services between the components modeled in the application and technology layers, and wherein the constructed proposed information system architecture further comprises an application bus, the application bus providing a communication, distribution, and management interface between application component models in the application layer;"

Hartley teaches technology bus as virtual machine (Hartley: at least in Col 10, Lines 24-31) and application bus as message buses (Hartley: at least in Col. 11, Lines 46-48, 63-65) as means for interfacing between different layers, in broader terms buses are considered to be data conduits between different layers.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take White's teaching and apply them to EUROEXPERT - Best Practices GATE model disclosed above to create a tool for improving quality in business process design. The motivation to do so would be a system than can be simulated with various components to meet the requirements. Six-sigma process is disclosed as a way of doing business (White: Pg 28, Col. 1, A.

What is Six Sigma, Line 6-9) to increase quality & attain competitive pricing (White: Pg 28, Col. 2, B "Why Pursue Six Sigma?" Line 1-6).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to use the layering approach, communication strategy and real-time/batch processing taught by Hartley and apply them to White/EUROEXPERT references. The motivation would be a design, which is abstract enough than can handle new business requirements without significantly changing the underlying architecture, and specific enough that the business layer can provide rule based processing by passing in metadata. Hence, the business model would be extremely adaptive to changing business, application & technological requirements.

Regarding Claim 2

As disclosed above, White proposes performance matrix modification, update and comparison (White: Pg 34, Col. 1, 1-6 & Figure 4). He discloses the circuit component that gives the best results for the quality/cost level (White: Pg 34, Col. 2, 1-3 & Table V). White further discloses a matrix of components with various tolerances and how they are used to access the performance of the circuit (White: Pg 33, Figure 3 & Pg 34, Table V & VI). The output of his analysis is selection of the component, which is least expensive and highest quality (White: Pg 34, Col. 2, 1-3).

Regarding Claim 3

As disclosed above, White identifies, evaluates various components required in the circuit (White: Pg 33, Col. 1, Figure 3). Searching the data store for various

components is implicit, as he has already identified the all variations with different tolerances (White: Pg 33, Col. 1, Table 2).

Regarding Claim 4

White suggests that replacement of components be done one at a time to accurately calculate improved performance (White: Pg 34,Col. 1, F Step 5, Line 1-8 & Table V).

Regarding Claim 5

EUROEXPERT & White do not teach modifying the business model if the supporting components models in application and technology layers have unacceptable performance metrics. However, It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to modify the business model when the supporting components models are not able to meet performance as it is well-known in the art that business model need to be changed when the underlying application or technology is unable to support the business goals.

Regarding Claim 9

Disclosures for EUROEXPERT - Best Practices GATE model and White do not teach real-time and batch processing systems.

Hartley teaches business application layer (Hartley: at least in Col.5 lines 42-58) and an application engines layer (Hartley: at least in Col.3 Lines 52-67). Hartley exemplarily discloses applications design that respond in real time (Hartley: Col. 13, Lines 24-31) and another one, which is, batch process driven. Batch processing example disclosed is collection of customer charges (Hartley: Col. 17 Lines 58-68) & batch report generation (Hartley: Col. 19, Lines 18-23).

Regarding Claim 10

White discloses taking other models and values for the subcomponents to enhance performance and meet performance (White: Pg 34,Col. 1, F Step 5, Line 1-8 & Table V).

Regarding Claim 11

Claim 11 is rejected for the same reasons as claims 1, 2 & 9 are rejected. Further Hartley discloses a system that includes a rule-based engine (Hartley: Abstract Lines 12-15). The output module is the claim is equivalent to batch output component that is disclosed in Claim 9.

Specifically, EUROEXPERT teaches the limitation presented in step (a) and most of step (b) as a tiered model GATE model identical to claimed model application that collects measurements from 3 domains, namely, business domain/layer, application domain, technology/system/network domain, illustrated by a figure called "Modeling Business Value Chain" (EUROEXPERT Best Practices: Col 2), *representing an information system (EUROEXPERT: Fig on Pg.2) where each layer has different data than each other (EUROEXPERT: Fig on Pg.1)*. This model incorporates the business goals and characteristics of the system design. It can be seen from the reference that this model captures the business requirements for business processes as well as delegates them to 3 layers. The public knew about this model in February 1992 (EUROEXPERT Best Practices: Col 2, Lines 16-18). EUROEXPERT teaches constructing such a system ((EUROEXPERT: Approach Col 2 – Stage 2 completed in May 1992).

White teaches step (c) as modeling performance of the components and their variations using an electrical circuit example (White: Pg 33, Col. 1, D Step 3, Line 3-8; During construction – Pg. 35 Section H). These components can then be simulated to measure their performance using various mathematical & statistical calculation, White discloses circuit example with Monte Carlo simulation (White: Pg 33, Col 2, 2nd Paragraph).

White further teaches step (d) as comparing the results of a simulation against the expected values (White: Pg 34, Col. 1, 1-6 & Figure 4). The figure (White: Figure 4) disclosed shows the unacceptable performance as compared to the expected results.

Hartley teaches step (e) as a system that includes a rule-based engine (Hartley: Abstract Lines 12-15; Col.12 Line 62-Col.13 Line 7).

White teaches step (f) as replacing the instant model and taking other models & values for the sub-components to enhance and meet performance (White: Pg 34, Col. 1, F Step 5, Line 1-8 & Table V). Modifications are suggested after the results from these simulations are gathered – i.e., in the circuit example used components of higher tolerances are suggested (White: Pg 34, Col. 1, F Step 5, Line 15-16). The reference teaches narrower versions of broader claims in the application. Here a simple electric circuit example teaches an abstract methodology that can be applied to a much bigger multi-tiered system as claimed. Outputting the design, which EUROEXPERT teaches as stage 2 implementation of the model (EUROEXPERT: Pg.1, Fig. on Pg.2 "New functional Elements").

Harley teaches the remaining step (a) limitations regarding mapping buses (Hartley: Col. 5 Lines 12-32, also see Fig.4; Col.11 Lines 34-45; Col 10, Lines 50-55, Lines 64-67; Col. 8 Lines 11-16) and application & technology buses (Hartley: at least in Col 10, Lines 24-31 at least in Col. 11, Lines 46-48, 63-65).

The motivation to combine White with EUROEXPERT is same as provided in claim 1 rejection. Further, motivation to combine Hartley with EUROEXPERT-White is also provided in claim 1 rejection.

Regarding Claim 12

Claim 12 is rejected for the same reasons as claims 1, 2.

Regarding Claim 13

Claim 13 is rejected for the same reasons as claims 1, 2.

Regarding Claim 14

Claim 14 is rejected for the same reasons as claims 1.

Regarding Claim 15

Claim 15 is rejected for the same reasons as claims 5.

Regarding Claim 19

Claim 19 is rejected for the same reasons as claims 9.

Regarding Claim 20

Claim 20 is rejected for the same reasons as claims 10.

Regarding Claim 21

Claim 21 is rejected for the same reasons as claims 1 & 2.

Regarding Claim 22

Claim 22 is rejected for the same reasons as claims 1 & 2.

Regarding Claim 23

Claim 23 is rejected for the same reasons as claims 1.

Conclusion

14. All claims are rejected.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

16. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Thursday, January 18, 2007

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Supervisory Patent Examiner, GAU 2128
Structural Design, Modeling, Simulation and Emulation

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